LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor device having a plurality of thin film resistance elements located above an interlayer insulating film above an area where at least one of an element and a wire is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate is set to be within a range that is greater than 0° and less than or equal to 10°, wherein each of the plurality of thin film resistance elements has a similar shape, wherein the interlayer insulating film includes an inorganic spin-on-glass film and a tetraethylorthosilicate film covering a surface of the inorganic spin-on-glass film.

2. (Currently Amended) The semiconductor device according to claim 1, wherein the ~~interlayer insulating film comprises an~~ inorganic spin-on-glass film is formed so as to cover the overall area below the area where the plurality of thin film resistance elements is formed.

3. (Currently Amended) A semiconductor device having a plurality of thin film resistance elements located above an interlayer insulating film above an area where at least one of an element and a wire is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate is set to be within a range that is greater than 0° and less than or equal to 10°, wherein each of the plurality of thin film resistance

elements has a similar shape, wherein the interlayer insulating film includes an inorganic spin-on-glass film and a tetraethylorthosilicate film covering a surface of the inorganic spin-on-glass film, ~~The semiconductor device according to claim 1, wherein the interlayer insulating film comprises an inorganic spin-on-glass film, and~~ wherein an upper surface of the interlayer insulating film has a higher area adjacent to an area where the plurality of thin film resistance elements is formed than in the area where the plurality of thin film resistance elements is not formed.

4. (Currently Amended) The semiconductor device according to claim 1, wherein the plurality of thin film resistance elements is formed [[on]] above an area where [[the]] a plurality of wires ~~wire~~ is formed, and a wire interval is set to 1.7μm or more.

5. (Previously Presented) The semiconductor device according to claim 1, wherein the plurality of thin film resistance elements is formed above the area where the wire is formed, and the plurality of thin film resistance elements and the wire are disposed in parallel to each other so that projections thereof are overlapped with each other.

6. (Currently Amended) A semiconductor device having a plurality of thin film resistance elements located above an interlayer insulating film above an area where at least one of an element and a wire is formed, wherein the interlayer insulting film comprises an inorganic spin-on-glass film and a tetraethylorthosilicate film, wherein the inorganic spin-on-glass film is formed so as to cover the overall area below an area where the plurality of thin film resistance elements is formed, wherein each of the plurality of thin film resistance elements has a similar

shape, wherein the tetraethylorthosilicate film is formed to cover a surface of the spin-on-glass film.

7. (Withdrawn) A method of manufacturing the semiconductor device of claim 6, the method comprising:

rotationally coating an inorganic spin-on-glass film to form the inorganic spin-on-glass film as the interlayer insulating film above the area while flattening the upper surface of the inorganic spin-on-glass film; and

forming any one of the thin film resistance element and an insulating film constituting the interlayer insulating film on the inorganic spin-on-glass film flattened by the rotational coating.

8. (Withdrawn) A method of manufacturing a semiconductor device having a thin film resistance element through an interlayer insulating film above an area where at least one of an element and a wire is formed, the method comprising:

rotationally coating an inorganic spin-on-glass film to form the inorganic spin-on-glass film as the interlayer insulating film above the area while flattening the upper surface of the inorganic spin-on-glass film; and

forming any one of the thin film resistance element and an insulating film constituting the interlayer insulating film on the inorganic spin-on-glass film flattened by the rotational coating.

9. (Currently Amended) A semiconductor device having a plurality of thin film resistance elements disposed above an interlayer insulating film above an area where at least one of an

element and a plurality of wires ~~wire~~ is formed on a semiconductor substrate, wherein a taper angle at which a line connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate is set to be greater than 0° and less than or equal to 10°, wherein the interlayer insulating film comprises an inorganic spin-on-glass film and a tetraethylorthosilicate film, wherein the inorganic spin-on-glass film is formed so as to cover the overall area below the area where the thin film resistance element is formed, wherein the plurality of thin film resistance elements is formed on an area where the plurality of wires ~~wire~~ is formed, and a wire interval is set to 1.7μm or more, wherein each of the plurality of thin film resistance elements has a similar shape, wherein the tetraethylorthosilicate film is formed to cover a surface of the inorganic spin-on-glass film.

10. (Previously Presented) The semiconductor device according to claim 9, wherein each of the plurality of thin film resistance elements is formed to have a width in a range between 1 and 10μm, and a thickness in a range between 10 and 50nm.

11. (Previously Presented) The semiconductor device according to claim 3, wherein each of the plurality of thin film resistance elements is formed to have a width in a range between 1 and 10μm, and a thickness in a range between 10 and 50nm.

12. (Currently Amended) A semiconductor device having a plurality of thin film resistance elements disposed above an interlayer insulating film above an area where a plurality of wires is formed on a semiconductor substrate, wherein a taper angle at which a line

connecting the local maximum and minimum points of a step on the upper surface of the interlayer insulating film beneath an area where the plurality of thin film resistance elements is formed intersects to the surface of the semiconductor substrate is set to be greater than 0° and less than or equal to 10°, wherein the interlayer insulating film comprises an inorganic spin-on-glass film and a tetraethylorthosilicate film covering a surface of the inorganic spin-on-glass film, wherein a wire interval is set to 1.7μm or more, wherein each of the plurality of thin film resistance elements has a similar shape.

13. (Previously Presented) The semiconductor device according to claim 1, wherein the plurality of thin film resistance elements further comprises paired thin film resistance elements.

Claims 14 - 15 (Canceled)

16. (Previously Presented) The semiconductor device according to claim 1, wherein each of the plurality of thin film resistance elements comprises chromium silicon.

17. (Previously Presented) The semiconductor device according to claim 6, wherein each of the plurality of thin film resistance elements comprises chromium silicon.